Abstract of the Disclosure:

In a semiconductor memory incorporating therein a circuit for relieving a defective memory cell, a memory cell array constituted of a number of main memory cells MC00 to MCij is added with one column of redundant memory cells MC0j+1 to MCij+1 and one word line of substitution information storing memory cells MCRA0 to MCRAj+1. In only a first cycle after the power supply is turned on, the substitution information DR0 to DRj is read out from the substitution information storing memory cells by use of a writing/reading circuit associated with the main memory cells, and is transferred to and held in a control circuit. In a second and succeeding cycles, the control circuit generates Y selection circuit control signals CS0 to CSj on the basis of the substitution information held in the control circuit, and a Y selection circuit is controlled by the control signals CS0 to CSj so as to selectively connect the columns other than a defective column to an input/output line. Thus, a chip area overhead attributable to the installation of the defective memory cell relief circuit is minimized. In addition, an address comparing circuit for a defective memory cell substitution is no longer necessary, and an access time overhead attributable to the address substitution operation does not occur.

Fig. 1